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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ANDERS LANDIN and ERIK E. HAGERSTEN

Appeal 2009-005677
Application 10/821,412[1]
Technology Center 2100

Before LANCE LEONARD BARRY, JAY P. LUCAS and
ST. JOHN COURTENAY III, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge*.

DECISION ON APPEAL[2]

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[1] Application filed April 9, 2004. The real party in interest is Sun Microsystems, Inc.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or for filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the "MAIL DATE" (paper delivery mode) or the "NOTIFICATION DATE" (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF THE CASE

Appellants appeal from a final rejection of claims 1 to 38 under authority of 35 U.S.C. § 134(a). The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellants' invention relates to a method for reading data in a multi-node system while maintaining coherency across nodes. In the words of Appellants:

> Independent claim 1 is directed to a system (*See* e.g., FIG. 20, #100) including a node (*See* e.g., FIG. 20, #140A) and an additional node (*See* e.g., FIG. 20, #140B) coupled by an inter-node network (*See* e.g., FIG. 20, #154). The node includes an active device (*See* e.g., FIG. 20, #142A, 146A), an interface (*See* e.g., FIG. 20, #148A) to the inter-node network, a system memory (*See* e.g., FIG. 20, #144A), and an address network (*See* e.g., FIG. 20, #150A) and a data network (*See* e.g., FIG. 20, #152A) that is separate from the address network (*See* e.g., specification page 11, lines 18-20), coupling the active device, the interface, and the system memory. The active device sends an address packet to initiate a transaction to gain an access right to a coherency unit (*See* e.g., specification page 70, lines 13-17). In response to receiving the address packet, the system memory is configured to send a report corresponding to the address packet to the interface if the transaction cannot be satisfied within the node (*See* e.g., specification page 70, lines 10-21). The interface is configured to ignore the address packet and to send a coherency message requesting the access right to the additional node via the inter-node network in

response to the report (*See* e.g., specification page 70, lines 10-21; page 71, lines 9-14).

(App. Br. 6).

> In some embodiments, interfaces 148 may ignore address packets specifying LPA coherency units unless received in a special format. This may allow transactions that do not require coherency messages to other nodes to complete locally within a node without taking up resources within the interface and the inter-node network. However, in some cases (e.g., an RTO transaction initiated by an active device within a gS node for an LPA coherency unit), coherency messages to other nodes (e.g., to invalidate shared copies in other nodes) may be needed in order to complete a transaction for an LPA coherency unit. In those situations, a home memory subsystem may send a REP (Report) packet to an interface. The REP packet identifies the transaction involving the LPA coherency unit and indicates that the interface's intervention is needed to complete the transaction. Receipt of a REP packet may cause an interface to send coherency messages to interfaces in other nodes and/or to initiate one or more subtransactions.

(Spec. 70, ¶ [0194]).

The following illustrates the claims on appeal:

Claim 1:

1. A system, comprising:

a node including an active device, an interface to an inter-node network, a system memory, and an address network and a data network that is

separate from the address network, coupling the active device, the interface, and the system memory;

an additional node coupled to the node by the inter-node network;

wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the system memory is configured to send a report corresponding to the address packet to the interface if the transaction cannot be satisfied within the node;

wherein the interface is configured to ignore the address packet and to send a coherency message requesting the access right to the additional node via the inter-node network in response to the report.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Liencres	US 5,434,993	Jul. 18, 1995
Roy	US 6,065,092	May, 16, 2000
Chandrasekaran	US 6,970,872 B1	Nov. 29, 2005 (filed on Jul. 23, 2002)

REJECTIONS

The Examiner rejects the claims as follows:

Claims 1 to 38 stand rejected under 35 U.S.C. § 103(a) for being obvious over Liencres in view of Chandrasekaran and further in view of Roy.

ISSUE

The issue is whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 103(a). The issue specifically turns on whether the references Liencres, Chandrasekaran and Roy teach or suggest the use of a report from the node's system memory to permit an address packet to initiate a transaction from an interface to a coherency unit in another node.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellants have invented a method and system for maintaining coherency in a computer system comprising multiple nodes, so that the nodes are aware that data in a cache or other memory may be invalid (Spec. ¶ [0053]). Coherency units perform this task and are alerted to changes in state by coherency messages sent between interfaces in the nodes (¶ [0175]). Within the node, different types of packets on address busses alert the active devices of changes in ownership of the coherency units (¶ [0250]). Transactions that do not require coherency messages to

other nodes are ignored by the interface (¶ [0194]). However, when a coherency message to another node is needed, the system memory sends a report packet to the interface. On receipt of the report packet, the interface will send the coherency message (*id.*).

2. The Liencres reference teaches a multi-node computer system, containing cache control systems (col. 6, ll. 39 to 61). Cache lines contain status bits indicating if a cache line is valid, owned (modified and not written back to main memory yet) or shared (col. 3, ll. 50 to 55).

3. The Chandrasekaran reference teaches a technique for reducing latency in a multi-node system by "optimistically reading" data that is not in cache, on the chance that it will be valid (col. 6, ll. 25 to 36).

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

ANALYSIS

Arguments with respect to the rejection of claims 1 to 38 under 35 U.S.C. § 103(a) [R1]

The Examiner has rejected the noted claims for being obvious over Liencres in view of Chandrasekaran and Roy. Appellants have presented a number of arguments (App. Br. 9 to 14).

Appellants contend that the references, most notably the Chandrasekaran reference, fail to teach key limitations of the independent claims 1, 14 and 26. Chandrasekaran was cited by the Examiner for teaching the limitation "wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the system memory is configured to send a report corresponding to the address packet to the interface if the transaction cannot be satisfied within the node; wherein the interface is configured to ignore the address packet and to send a coherency message requesting the access right to the additional node via the inter-node network in response to the report." (Ans. 5, top). Chandrasekaran teaches write time validity checking of data in a cache wherein the time of a read from cache is validated if it was started after the last write (i.e., the data is still valid since new data was not sent to overwrite the data in cache) (col. 6. l. 28). Thus when writing, a node must publish its write time so it can be compared to the read time (*id.*).

The Examiner is reading this publication of the write time as the claimed report (Ans. 5, top). However, in the claim the report is sent by the system memory "if the transaction cannot be satisfied within the node." (claim 1). The reference does not teach or suggest the claimed node, the sending of address packet within the node, the ignoring of that address

packet unless a message is sent to an interface, and the communication by that interface to a coherency unit in an additional node. We see the similarity noted by the Examiner of the conditional-read mechanism, depending on the timing, but the other elements of the claim are not present or suggested either in Chandrasekaran or in Liencres operating as claimed. We thus agree with the Appellants that the references do not contain sufficient teachings to render obvious the independent claims.

We find that the Appellants have shown error in the Examiner's rejection, which reaches all of the claims.

CONCLUSIONS OF LAW

Based on the findings of facts and analysis above, we conclude that Appellants have shown that the Examiner erred in rejecting claims 1 to 38.

DECISION

We reverse the Examiner's rejection of claims 1 to 38 under 35 U.S.C. § 103(a).

REVERSED

peb

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